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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,488	04/16/2004	Eric Jeffrey	VP115	1354

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EPSON RESEARCH AND DEVELOPMENT INC  
INTELLECTUAL PROPERTY DEPT  
2580 ORCHARD PARKWAY, SUITE 225  
SAN JOSE, CA 95131

EXAMINER
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ALMEIDA, CORY A

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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03/03/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/826,488	<b>Applicant(s)</b> JEFFREY ET AL.	
	<b>Examiner</b> CORY A. ALMEIDA	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 7-11, and 13-18, are rejected under 35 U.S.C. 102(b) as being anticipated by Willis 5329369.

3. In regards to claim 1 and the associated claim 15, Willis discloses a method for displaying an image in an electronic medium (Abstract), comprising a register (Abstract, video memory and Col. 13 12-35), changing a first set of dimension values associated with an image being displayed, wherein the image being displayed remains undisturbed when changing the first set of dimension values (Col. 12, 11-32), changing a second set of dimension values associated with a display region in which the image is being displayed, wherein the display region remains undisturbed when changing the second set of dimension values (Col. 12, 33-53), providing a completion signal indicating completion of changing the first set of dimension values and the second set of dimension values (Col. 12, 21-53 discloses changing sizes of both video signals which means that after they are changed they would be completed), receiving a trigger signal indicating a beginning of a new image to be displayed (Col. 6, 50 – Col. 7, 6), and implementing the changed first set of dimension values and the changed second set of

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dimension values upon receiving the trigger signal while the completion signal is being provided (Col. 21, 30-35).

4. In regards to claim 2, Willis discloses changing the first set of dimension values and the second set of dimension values spans a number of trigger signal receptions while the completion signal has not yet been provided (Col. 12, 21-53 discloses changing sizes of both video signals which includes a finite amount of time before it is completed).

5. In regards to claim 3, Willis discloses operating image synchronization logic to recognize receipt of the trigger signal while the completion signal is being provided, and operating the image synchronization logic to cause an essentially simultaneous implementation of the changed first set of dimension values and the changed second set of dimension values (Col. 21, 30-35).

6. In regards to claim 7, Willis discloses the image is a camera image (Col. 2, 5-29) and the trigger signal is a VSYNC signal indicating a new frame of the camera image (Col. 11, 38-51).

7. In regards to claim 8 and associated claim 13, Willis discloses a method for displaying a live camera image in a picture-in-picture (PIP) window (Col. 2, 5-29), comprising a register (Abstract, video memory and Col. 13 12-35), receiving an input to change a size of the PIP window (Col. 12, 46-53), changing a value stored in a PIP window dimension register (Col. 12, 46-53), changing a value stored in a camera image dimension register (Col. 13, 21-53), setting an enable bit to indicate a completion of changing the values stored in the PIP window dimension register and the camera image

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dimension register (Col. 12, 21-53 discloses changing sizes of both video signals which means that after they are changed they would be completed), receiving a new frame signal associated with the camera image (Col. 6, 50 – Col. 7, 6), and implementing the values stored in the PIP window dimension register and the camera image dimension register upon receiving the new frame signal, wherein implementing the values is enabled by the enable bit being set to indicate a completion of changing the values stored in the PIP window dimension register and the camera image dimension register (Col. 12, 21-53 and Col. 21, 30-35).

8. In regards to claim 9, Willis discloses delaying implementation of the changed values stored in the PIP window dimension register and the camera image dimension register until the new frame signal is received while the enable bit is set to indicate a completion of changing the values (Col. 12, 21-53 discloses changing sizes of both video signals which includes a finite amount of time or frames before it is completed).

9. In regards to claim 10, Willis discloses changing the values stored in the PIP window dimension register and the camera image dimension register spans a number of new frame signals while the enable bit has not yet been set (Col. 12, 21-53 discloses changing sizes of both videos which includes a finite amount of time or frames before it is completed).

10. In regards to claim 11, Willis discloses the new frame signal associated with the camera image is a VSYNC signal (Col. 11, 38-51).

11. In regards to claim 14, Willis discloses maintaining implementation of previous values stored in the dimension registers when receiving the signal indicating the

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beginning of the new camera image frame when each enable bit indicates an incomplete status of the dimension register changes (Col. 12, 21-53 discloses changing sizes of both videos would include maintaining current values of sizes until a resize is complete so the user doesn't see non-complete video data on screen).

12. In regards to claim 16, Willis discloses the image synchronization circuitry is configured to recognize a vertical synchronization signal as the trigger signal, the vertical synchronization signal to be provided in conjunction with image data to be received by the display controller (Col. 11, 38-51).

13. In regards to claim 17, Willis discloses the image synchronization circuitry is configured to implement the dimension values stored in each of the first set of dimension registers and the second set of dimension registers in a simultaneous manner (Col. 2, 42-64).

14. In regards to claim 18, Willis discloses camera interface circuitry configured to receive data defining the image to be displayed (Col. 11, 32-51), and resizer circuitry configured to adjust a size of the image to be displayed in accordance with dimension values stored in the first set of dimension registers, the resizer circuitry further configured to be controlled by the image synchronization circuitry (Col. 12, 21-53).

### ***Claim Rejections - 35 USC § 103***

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 4-6, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis 5,329,369.

17. In regards to claim 4, Willis discloses a video ram or memory (Abstract, video memory and Col. 13 12-35).

Willis does not disclose expressly the first set of dimension values are stored in four registers associated with camera image resizer logic and the second set of dimension values are stored in four registers associated with a picture-in-picture (PIP) window.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art that the dimension values for the main camera window and the pip window could be stored in 4 separate registers or one main memory as Willis discloses without diverting from the scope of the invention.

The motivation for doing so would have been simplification of parts.

Therefore, it would have been obvious that Willis discloses the invention of claim 4.

18. In regards to claim 5, Willis discloses a video ram or memory (Abstract, video memory and Col. 13 12-35).

Willis does not disclose expressly providing the completion signal is performed by setting an enable bit within a last register changed, wherein the last register changed represents a final register required to have its dimension value changed.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art that a write enable or completion bit could be stored in the memory Willis discloses.

The motivation for doing so would have been for error prevention.

Therefore, it would have been obvious that Willis discloses the invention of claim 5.

19. In regards to claim 6, Willis discloses a video ram or memory (Abstract, video memory and Col. 13 12-35).

Willis does not disclose expressly changing the first set of dimension values stored in the four registers associated with camera image resizer logic is performed by duplicating changes made to the second set of dimension values stored in the four registers associated with the PIP window.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art that one could duplicate dimension values from one memory location to another to make the main window and PIP window the same size.

The motivation for doing so would have been for showing two images with equal focus as shown in Willis Fig. 1d.

Therefore, it would have been obvious that Willis discloses the invention of claim 6.

20. In regards to claim 12, Willis discloses a video ram or memory (Abstract, video memory and Col. 13 12-35).

Willis does not disclose expressly each PIP window dimension register and each camera image dimension register includes the enable bit, the enable bit being set in a last dimension register to be changed upon completion of the change in the last dimension register.

However, at the time of the invention, it would have been obvious to one of ordinary skill in the art that a write enable or completion bit could be stored in the memory Willis discloses.

The motivation for doing so would have been for error prevention.

Therefore, it would have been obvious that Willis discloses the invention of claim 12.

21. Claims 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Willis 5,329,369 in view of Duhault, US-6456334.

22. In regards to claim 19, Willis does not disclose expressly the display controller is incorporated into a portable electronic computing device.

Duhault discloses a multiple window or PIP laptop (Fig. 1, Col. 1 41-45 and Col. 2 16-31).

At the time of the invention it would have been obvious that the PIP device of Willis could be incorporated into a device such as a laptop as Duhault discloses.

The motivation would have been to present multiple images to a user simultaneously in a smaller form factor such as a laptop.

Therefore it would have been obvious to combine Duhault with Willis to obtain the invention as specified in claim 19.

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23. In regards to claim 20, Duhault discloses the portable electronic computing device is selected from the group consisting of a cellular phone, a personal digital assistant, a web tablet, and a pocket personal computer (Col. 2, 16-31).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CORY A. ALMEIDA whose telephone number is (571) 270-3143. The examiner can normally be reached on Monday through Friday 8AM to 4PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bipin Shalwala/  
Supervisory Patent Examiner, Art Unit 2629

CA

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